Remarks

Applicant respectfully requests reconsideration and reexamination. This amendment affects the claims of the above-identified application as follows:

- Claims 1, 2, 4, 8, 12, and 20 have been amended;
- Claims 10 and 11 have been canceled.

The Examiner has objected to the drawings for not indicating that Fig. 1 is prior art. Applicants have provided a marked-up copy of Fig. 1 herewith, along with a separate letter to the Official Draftsperson and a revised Fig. 1. Accordingly, this objection should be overcome.

The Examiner has objected to the claims for including the abbreviations "TX" and "RX" in referring to a "TX line" and to an "RX line." Applicants have amended each of the remaining claims that include either objected-to term (i.e., each of claims 1, 2, 4, 8, 12, and 20), to replace all instances of "TX" with the word "transmit" and to replace all instances of "RX" with word "receive." Therefore, this objection should be overcome. These changes are merely matters of form and are not intended to affect the scope of the respective claims.

The Examiner has rejected all of the claims (claims 1-20) under 35 U.S.C. § 102(b) as being anticipated by Ramamurthy et al. (U.S. Patent No. 5,790,563, hereinafter, "Ramamurthy"). Ramamurthy discloses a method for performing a self-test function an integrated circuit having a transmitter and a receiver. The test method appears to overcome certain problems associated with unpredictable latency of the receiver. See abstract.

As shown in Fig. 2, Ramamurthy's self-test circuit includes a transmitter 12 and a receiver 14, which respectively transmit and receive parallel data. A serializer 16 converts parallel data from the transmitter 12 to serial data, which may then be output via line 20. Line 20 is connectable to line 22, which is then input to a de-serializer 18. The de-serializer 18 converts the serial bit stream on line 22 to a parallel bit stream, which is then received by the receiver 14. A comparison unit 38 is coupled to the receiver 14, and may perform parametric testing on the parallel digital signal received by the receiver 14. Col. 5, lines 16-28.

The Examiner has rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated

by Ramamurthy. Claim 1 as amended is directed to a circuit for testing serial ports. The circuit includes a receiver, a transmitter, and a parametric measurement circuit. Significantly, the parametric measurement circuit is "coupled to the input of the receiver, for evaluating steady-state characteristics of the transmit line of the serial port."

Ramamurthy does not teach or suggest this aspect of claim 1 as amended. The comparison unit 38 of Ramamurthy is coupled to the output of the receiver 14. It is not "coupled the input of the receiver, for evaluating steady-state characteristics of the transmit line of the serial port."

This distinction is significant. Ramamurthy is concerned with testing the functionality of an integrated circuit as part of a self-test arrangement. To this end, the comparison unit 38 performs parametric testing on the de-serialized parallel data coming out of the receiver 14.

In contrast with Ramamurthy, the parametric measurement circuit of claim 1 as amended is concerned with "evaluating steady-state characteristics of the transmit line of the serial port" itself. In automatic test systems, it is desirable to evaluate signals that flow between devices, such as between a test system and a device under test. The parametric measurement circuit is preferably used for evaluating these signals, which are generally indicative of the performance of the device under test.

Accordingly, Ramamurthy does not anticipate claim 1 as amended, and the rejection of claim 1 as amended under 35 U.S.C. § 102(b) should be withdrawn.

Claims 2-7 depend from claim 1 as amended. Therefore, the rejections of each of claims 2-7 under 35 U.S.C. § 102(b) should also be withdrawn.

The Examiner has rejected claim 8 under 35 U.S.C. § 102(b) as being anticipated by Ramamurthy. Claim 8 as amended is directed to a circuit for testing serial ports in an automatic test system, and recites a receiver, a transmitter, and a time distortion circuit. The time distortion circuit is "interposed between the output of the receiver and the input of the transmitter, for introducing predetermined timing distortions into the test signal provided to the receive line of the serial port."

Ramamurthy does not teach or suggest this aspect of claim 8 as amended. Ramamurthy does not disclose the use of a "time distortion circuit." This difference is significant. The time distortion circuit recited in claim 8 as amended allows predetermined timing distortions (for example, jitter) to be introduced into a test signal, to improve the quality of testing.

Ramamurthy does not anticipate claim 8 as amended, and the rejection of claim 8 as amended under 35 U.S.C. § 102(b) should be withdrawn.

Claim 9 depends from claim 8 as amended. Therefore, the rejection of claim 9 under 35 U.S.C. § 102(b) should also be withdrawn.

The Examiner has rejected claim 12 under 35 U.S.C. § 102(b) as being anticipated by Ramamurthy. Claim 12 as amended is directed to a method of testing a serial port of a device under test, and is included below in its entirety:

> 12. A method of testing a serial port of a device under test in an automatic test system, comprising:
>
> (A) evaluating steady-state characteristics of at least one of a transmit line and a receive line of the serial port;
>
> (B) configuring the device under test to generate a serial bit stream;
>
> (C) receiving the serial bit stream from the transmit line of the serial port of the device under test;
>
> (D) transmitting one of the received serial bit stream and a direct input to the receive line of the serial port of the device under test; and
>
> (E) monitoring the device under test to determine whether the serial bit stream received by the device under test matches an expected serial bit stream.

Ramamurthy does not teach or suggest claim 12 as amended. As an initial matter, Ramamurthy is directed to a self-test method, wherein a semiconductor device is constructed and arranged for testing itself. Col. 1, lines 10-13. In contrast, claim 12 as amended is directed a test method involving at least two elements: a device under test and an automatic test system.

In addition, Ramamruthy does not teach or suggest step (A) of "evaluating steady-state characteristics of at least one of a transmit line and a receive line of the serial port." Ramamurthy appears to disclose a comparison unit 38 for performing parametric testing on a parallel digital signal (output of Rx 14). For reasons similar to those given above in connection with claim 1, however, this is different from "evaluating steady-state characteristics of at least one of a transmit line and a receive line of the serial port," as recited in claim 12 as amended.

Therefore, for at least these reasons, claim 12 as amended is not anticipated by

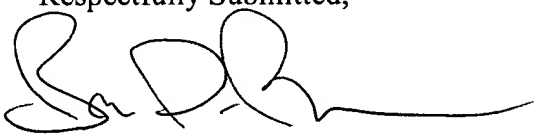
Ramamurthy, and the rejection of claim 12 under 35 U.S.C. § 102(b) should be withdrawn.

Claims 13-20 depend from claim 12 as amended. Therefore, the rejections of claims 13-20 under 35 U.S.C. § 102(b) should also be overcome.

Conclusion:

Applicants contend that the application is now in condition for allowance. A notice to that effect is earnestly solicited.

Respectfully Submitted,



Bruce D. Rubenstein
Reg. No. 39,349
Attorney for Applicant

Atty. Docket : 1473-US
Telephone : 617-422-3532
Fax : 617-422-2290

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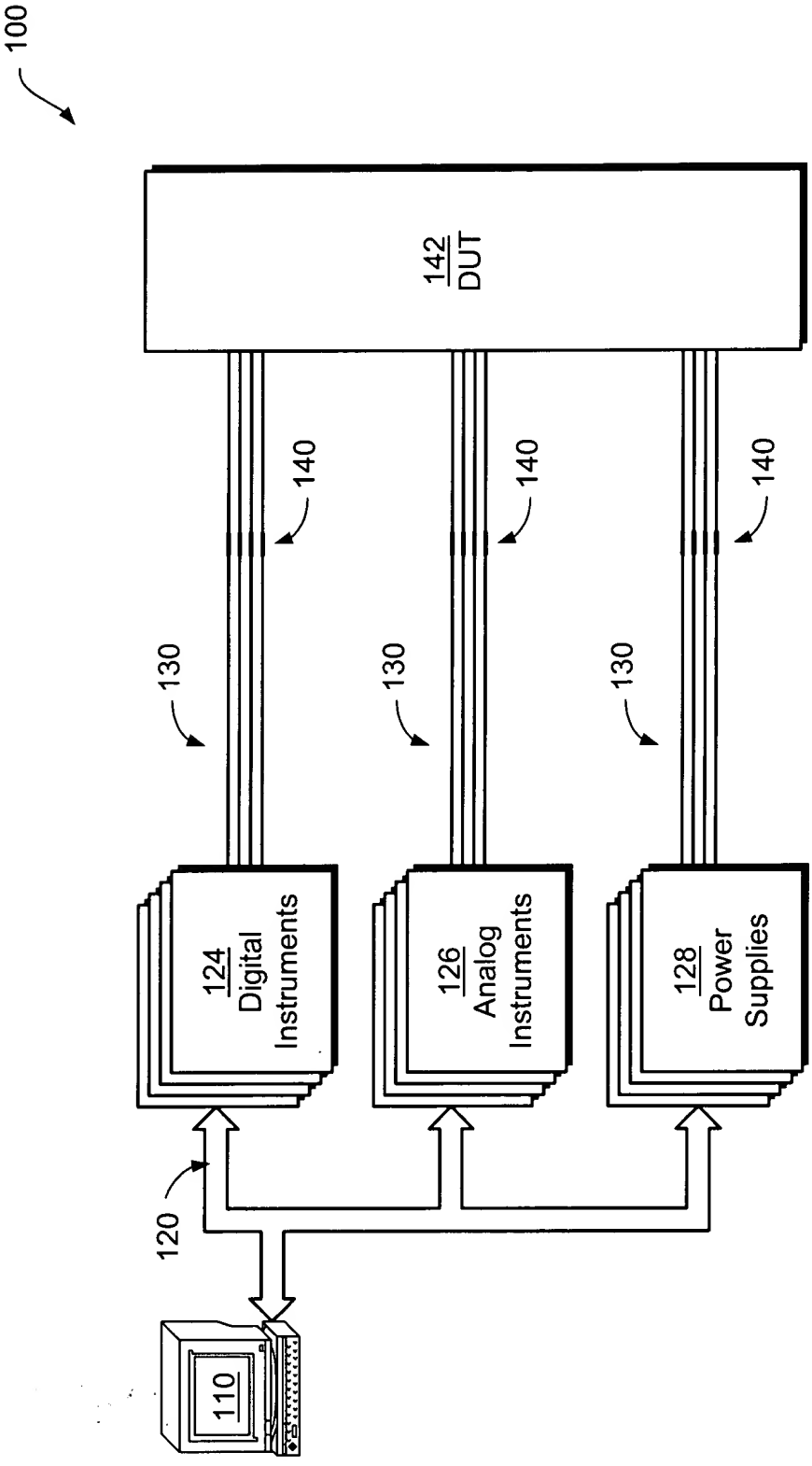

Fig. 1
(Prior Art)